WHAT IS CLAIMED IS:

1. A semiconductor apparatus comprising:

a processor having an instruction register inside thereof;

a pseudorandom number generating device,

the pseudorandom number generating device activated in response to a test operation and generating pseudorandom numbers; and

an input switchover device,

the input switchover device switching over between data input in normal operation and input of the pseudorandom numbers from the pseudorandom number generating device in the test operation to thereby output the data or pseudorandom numbers to the instruction register.

2. A semiconductor apparatus as claimed in Claim 1 further comprising,

an instruction converting device between the pseudorandom number generating device and input switchover device,

the instruction converting device outputting the pseudorandom numbers without change when the pseudorandom numbers inputted from the pseudorandom number generating device are defined instructions, and

converting the pseudorandom numbers into the defined instructions when the pseudorandom numbers are undefined instructions to thereby output the defined instructions.

3. A semiconductor apparatus comprising:

a processor,

the processor having, inside thereof, an instruction register and a difficult-to-control circuit part difficult to control by merely setting pseudorandom numbers in the instruction register;

a pseudorandom number generating device,

the pseudorandom number generating device activated in response to a test operation and generating pseudorandom numbers;

an input switchover device,

the input switchover device switching over between data input in normal operation and input of the pseudorandom numbers from the pseudorandom number generating device in the test operation to thereby output the data or pseudorandom numbers to the instruction register; and

a scan shift controlling device,

the scan shift controlling device scan inputting the pseudorandom numbers from the pseudorandom number generating device to the difficult-to-control circuit part in the test operation, and

scan outputting data from the difficult-to-control circuit part.

4. A semiconductor apparatus as claimed in claim 3 further comprising,

an instruction converting device between the pseudorandom number generating device and input switchover device,

the instruction converting device outputting the pseudorandom numbers without change when the pseudorandom numbers inputted from the pseudorandom number generating device are defined instructions, and

converting the pseudorandom numbers into the defined instructions when the pseudorandom numbers are undefined instructions to thereby output the defined instructions.

5. A semiconductor apparatus comprising:

a processor having an instruction register inside thereof;

a pseudorandom number generating device,

the pseudorandom number generating device activated in

response to a test operation and generating pseudorandom numbers;

a store instruction issuing device,

the store instruction issuing device periodically issuing store instructions for outside of an internal register;

a front input switchover device,

the front input switchover device switching over between the pseudorandom numbers from the pseudorandom number generating device and the store instructions from the store instruction issuing device in a test operation to thereby output the pseudorandom numbers or the store instructions; and

a rear input switchover device

the rear input switchover device switching over between data input in normal operation and input from the front input switchover device in the test operation to thereby output the data or the input from the front input switchover device to the instruction register.

6. A semiconductor apparatus comprising:

a processor having an instruction register inside thereof;

a pseudorandom number / store instruction issuing device,

the pseudorandom number / store instruction issuing device activated in response to a test operation and switching over between pseudorandom numbers and store instructions for outside of an internal register to thereby issue the pseudorandom numbers or the store instructions; and

an input switchover device,

the input switchover device switching over between data input in normal operation and input from the pseudorandom number / store instruction issuing device in the test operation to thereby output the data or the input from the front input switchover device to the instruction register.

7. A semiconductor apparatus as claimed in Claim 6 further

comprising:

a data compressing device on the output side of the internal registers,

the data compressing device compressing values in the internal registers to thereby output the compressed data to outside in response to the store instructions.